CLAIMS

What is claimed is:

1. An integrated circuit having an internal circuit and an external terminal for communicating between the internal circuit and circuitry external to the integrated circuit, the external terminal for receiving a supply voltage from the circuitry external to the integrated circuit, comprising:

a device for isolating the internal circuit from the external terminal, the device comprising:

control circuitry for sensing a short in the internal circuit and outputting a control signal in response thereto, the control circuitry including one of circuitry for sensing current drawn by the internal circuit exceeding a predetermined threshold and for outputting a control signal in response thereto, circuitry for sensing a voltage applied to the internal circuit below the predetermined threshold and for outputting the control signal in response thereto, and circuitry for sensing a voltage applied to the internal circuit above the predetermined threshold and for outputting the control signal in response thereto, the control circuitry comprising:

a first PMOS transistor having a source coupled to a supply terminal, a gate coupled to an output terminal, and a drain coupled to a control signal terminal;

a first resistive device coupled between the supply terminal and the output terminal;

a second resistive device coupled between the control signal terminal and a reference voltage bond pad;

a second PMOS transistor having a source coupled to the supply terminal, a gate, and a drain coupled to the control signal terminal;

an inverter coupled between the control signal terminal and the gate of the second PMOS transistor; and

circuitry for sensing a voltage applied to the internal circuit; and

switching circuitry coupled to the control circuitry for isolating the internal circuit from the external terminal in response to receiving the control signal.

2. The integrated circuit of claim 1, wherein the external terminal comprises a supply voltage bond pad for receiving the supply voltage from the circuitry external to the integrated circuit, wherein the supply terminal is coupled to the supply voltage bond pad for receiving the supply voltage, the output terminal for outputs the received supply voltage, and the control signal terminal for outputs the control signal in response to a current flow between the supply terminal and the output terminal exceeding the predetermined threshold.

3. The integrated circuit of claim 1, wherein the control circuitry for sensing a voltage further comprises circuitry for sensing a voltage applied to the internal circuit below the predetermined threshold and for outputting the control signal in response thereto.

4. The integrated circuit of claim 1, wherein the control circuitry further comprises circuitry for sensing a voltage applied to the internal circuit above the predetermined threshold and for outputting the control signal in response thereto.

5. An integrated circuit in a semiconductor memory die having at least one array of memory cells comprising:

an external communications terminal including a supply voltage bond pad;

an internal memory circuit;

switching circuitry coupled between the external communications terminal and the internal memory circuit for selectively isolating the internal memory circuit from the external communications terminal in response to receiving a control signal; and

control circuitry coupled to the external communications terminal and the switching circuitry for sensing a short in the internal memory circuit and outputting the control signal to the switching circuitry in response thereto, the control circuitry including one of circuitry for sensing current drawn by the internal circuit exceeding a predetermined threshold and for outputting a control signal in response thereto, circuitry for sensing a voltage applied to the internal circuit below the predetermined threshold and for outputting the control signal in response thereto, and circuitry for sensing a voltage applied to the internal

circuit above the predetermined threshold and for outputting the control signal in response thereto, the short-sensing control circuitry comprising:

a first PMOS transistor having a source coupled to a supply terminal, a gate coupled to an output terminal, and a drain coupled to a control signal terminal;

a first resistive device coupled between the supply terminal and the output terminal;

a second resistive device coupled between the control signal terminal and a reference voltage bond pad;

a second PMOS transistor having a source coupled to the supply terminal, a gate, and a drain coupled to the control signal terminal;

an inverter coupled between the control signal terminal and the gate of the second PMOS transistor; and

circuitry for sensing a voltage applied to the internal memory circuit.

6. The integrated circuit of claim 5, wherein the internal memory circuit is selected from a group of circuits comprising a Dynamic Random Access Memory (DRAM) circuit and a Static RAM (SRAM) circuit.

7. A semiconductor wafer having a plurality of integrated circuits in a plurality of semiconductor dice on the semiconductor wafer, each integrated circuit of the plurality comprising:

an external communications terminal for connecting to a supply voltage;

an internal memory circuit;

switching circuitry coupled between the external communications terminal and the internal memory circuit for selectively isolating the internal memory circuit from the external communications terminal in response to receiving a control signal; and

control circuitry coupled to the external communications terminal and the switching circuitry for sensing a short in the internal memory circuit and outputting the control signal to the switching circuitry in response thereto, the control circuitry including one of circuitry for sensing current drawn by the internal circuit exceeding a predetermined threshold and for

outputting a control signal in response thereto, circuitry for sensing a voltage applied to the internal circuit below the predetermined threshold and for outputting the control signal in response thereto, and circuitry for sensing a voltage applied to the internal circuit above the predetermined threshold and for outputting the control signal in response thereto, the short-sensing control circuitry comprising:

a first PMOS transistor having a source coupled to a supply terminal, a gate coupled to an output terminal, and a drain coupled to a control signal terminal;

a first resistor coupled between the supply terminal and the output terminal;

a second resistor coupled between the control signal terminal and a reference voltage bond pad;

a second PMOS transistor having a source coupled to the supply terminal, a gate, and a drain coupled to the control signal terminal;

an inverter coupled between the control signal terminal and the gate of the second PMOS transistor; and

circuitry for sensing a voltage applied to the internal circuit.

8. A method for isolating and testing integrated circuits in each of a plurality of semiconductor dice on a semiconductor wafer, the method comprising:

providing control circuitry within each semiconductor die of the plurality for sensing a short in an integrated circuit of the plurality of semiconductor dice, the control circuitry including one of circuitry for sensing current drawn by the internal circuit exceeding a predetermined threshold and for outputting a control signal in response thereto, circuitry for sensing a voltage applied to the internal circuit below the predetermined threshold and for outputting the control signal in response thereto, and circuitry for sensing a voltage applied to the internal circuit above the predetermined threshold and for outputting the control signal in response thereto, the control circuitry comprising:

a first PMOS transistor having a source coupled to a supply terminal, a gate coupled to an output terminal, and a drain coupled to a control signal terminal;

a first resistive device coupled between the supply terminal and the output terminal;

a second resistive device coupled between the control signal terminal and a reference voltage bond pad;

a second PMOS transistor having a source coupled to the supply terminal, a gate, and a drain coupled to the control signal terminal; an inverter coupled between the control signal terminal and the gate of the second PMOS transistor;

circuitry for sensing a voltage applied to the internal circuit; and

testing the plurality of semiconductor dice so that when the control circuitry in one of the plurality of semiconductor dice under test senses a short, automatically switching and isolating an integrated circuit having the short in the one of the plurality of semiconductor dice from other integrated circuits in the plurality of semiconductor dice.

9. The method of claim 8, wherein providing control circuitry comprises providing control circuitry within each semiconductor die of the plurality of semiconductor dice for sensing current drawn by the integrated circuit in a semiconductor die of the plurality that exceeds a predetermined threshold.

10. The method of claim 8, wherein providing control circuitry comprises providing control circuitry within each semiconductor die of the plurality for sensing a voltage within the integrated circuit in a semiconductor die of the plurality of semiconductor dice that is below a predetermined threshold.

11. The method of claim 8, wherein providing control circuitry comprises providing control circuitry within a semiconductor die of the plurality of semiconductor dice for sensing a voltage within the integrated circuit in the semiconductor die of the plurality that is above a predetermined threshold.

12. The method of claim 8, wherein testing the plurality of semiconductor dice comprises probe testing the plurality of semiconductor dice.

13. The method of claim 8, wherein isolating the integrated circuit having the short in the one of the plurality of semiconductor dice from the other integrated circuits of the plurality of semiconductor dice comprises opening a switch in the integrated circuit having the short that couples internal circuitry therein to the other integrated circuits in the plurality of semiconductor dice.